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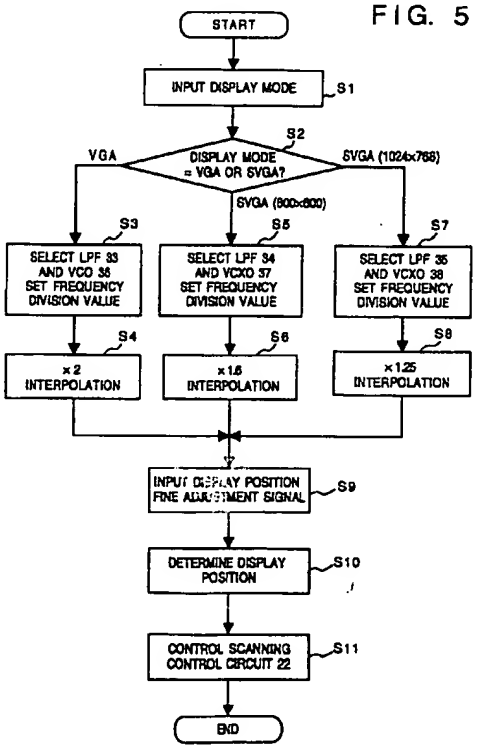
(54) Display mode detector, pixel clock synchroniser and interpolator for ferroelectric liquid crystal display

(57) A display control apparatus for displaying an image by receiving an RGB video signal including an image signal and a synchronizing signal receives horizontal and vertical synchronizing signals in the RGB video signal, and detects the current display mode using a display mode detector. A pixel synchronizing clock signal is generated using a clock generator in correspondence with the detected display mode, and the RGB video signal is interpolated by an interpolation processing circuit in correspondence with the display mode and the display screen size of an FLCD panel. The interpolated video signal is subjected to image signal processing, and the processed video signal is displayed on the FLCD panel.

FIG. 5



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Description

BACKGROUND OF THE INVENTION

The present invention relates to a display device for displaying an image on a screen, and a display control method and apparatus therefor.

In recent years, personal computers are widely used not only in processing of scientific and technical data, but also in applications requiring a graphic display such as CAD, design, and the like. Accordingly, it is required to improve the image quality and definition in the graphic display of a computer display. In order to meet such requirements, the following methods are available:

(1) to increase the display resolution; and
(2) to increase the frame (field) frequency. By the former method (1), a high-definition image can be obtained, and by the latter method (2), an image display free from flickering is attained.

Furthermore, recent personal computers normally use displays capable of a display operation in an SVGA (Super Video Graphic Array) mode at a high resolution of 800 x 600, 1,024 x 768, or 1,280 x 1,024 in addition to a VGA (Video Graphic Array) mode at a resolution of 640 x 480, which was the standard mode before the advent of the SVGA mode. In addition, the frequency of a vertical synchronizing signal used in the display is increasing from 60 Hz to more than 70 Hz. In this manner, the display performance of a personal computer is improving to a level as high as that of a workstation.

On the other hand, as a display device, a flat panel display using, e.g., a liquid crystal has recently received a lot of attention. It is expected that such a flat panel display be used as a display monitor not only for lap-top computers and notebook computers but also for desktop computers due to its compact structure and very low radiation of electromagnetic waves in place of CRT displays used so far.

As one of the flat panel displays, a display using a ferroelectric liquid crystal (FLC) (to be abbreviated as an FLCD hereinafter) is commercially available. Such an FLCD has a nature called a memory characteristic (i.e., a nature that maintains the ON/OFF states of liquid crystal pixels after an electric field required for turning on/off the pixels to be displayed is removed), and by utilizing this characteristic, a large-screen of flat panel display, which is very difficult to attain by the conventional liquid crystal technique, can be realized. More specifically, by using a partial rewrite scanning mode for selectively scanning only lines of changed image data to be displayed, the screen can be efficiently refreshed. With this technique, even when the frequency for rewriting the entire frame (to be simply referred to as a frame frequency hereinafter for the sake of simplicity) lowers due to an increase in number of display lines upon construction of a large-screen/high-definition display, a sufficient response speed can be assured as the screen of the computer display.

With the existing FLCD techniques, since each pixel to be displayed is set in either the ON or OFF state, a binary display is basically performed. For this reason, in order to obtain a larger numbed of display colors, one or a plurality of methods below must be independently used or combined.

(1) Each pixel is divided into sub-pixels, and area gradation is attained by combining the sub-pixels.
(2) Digital halftone processing such as the "dither method", the "error diffusion method", or the like is performed to attain pseudo halftone expression.

Furthermore, in the case of a display which changes the display state in real time, high-speed processing is required in the sub-pixel driving operation or the digital halftone processing.

When a video signal supplied from a computer is displayed on the screen of an FLCD of high-definition, the display operation is realized as follows. That is, when the number of display pixels of the FLCD is equal to the number of pixels output from the computer, i.e., is 1,280 x 1,024, image and synchronizing signal are received from the computer, and horizontal and vertical synchronizing signals are separated from the synchronizing signal. Using the separated horizontal synchronizing signal, FLCD dot clock signal synchronized with the pixel clocks of the computer is reproduced, and the image signal is A/D (analog-to-digital) converted using the FLCD dot clock signal. The converted digital data is subjected to γ characteristic adjustment and halftone processing. Thereafter, the digital image data is transferred to an output controller of the FLCD, thus displaying an image. In this case, the timings of the horizontal and vertical synchronizing signals and the dot clock signal synchronized with displaying pixels are peculiar to each computer. For this reason, using an FLCD interface board depending on a computer to be connected, image data from the computer can be displayed on the FLCD.

However, when an image signal from the computer is displayed on the FLCD by the above-mentioned method, the following problems are posed.

(1) Since there are some display modes such as VGA, SVGA, and the like, FLCD dot clock signal used for A/D-converting image data must be reproduced in correspondence with each display mode. For this purpose, a plurality of display control circuits depending on the respective display modes are required, and loads associated with cost and limitations in use are imposed on a user.
(2) When display operations in the respective display modes are performed on the FLCD as a bit-map display, if the VGA mode is selected, the number of pixels of a video signal in the VGA mode is 640 x 480, and hence, an image is displayed only a portion about 1/4 of the 1,280 x 1,024 FLCD display. More

specifically, the features of the large-screen, high-definition FLCD cannot be fully utilized.

SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above situation, and has as its object to provide a display device which can display an image in correspondence with various display modes, and a display control method and apparatus therefor.

It is another object of the present invention to provide a display device which can display an image by effectively utilizing the display screen, and a display control method and apparatus therefor.

It is still another object of the present invention to provide a display device which can perform display control corresponding to various display modes using one display interface circuit, and a display control method and apparatus therefor.

It is still another object of the present invention to provide a display device which can display an input video signal in an enlarged scale in correspondence with the display mode and size of the input video signal, and the size of the display screen, and a display control method and apparatus therefor.

It is still another object of the present invention to provide a display device which can adjust the display position of an image on the display screen, and a display control method and apparatus therefor.

It is still another object of the present invention to provide a display device which can display an image in both the VGA and SVGA modes, and a display control method and apparatus therefor.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principle of the invention.

Fig. 1 is a block diagram showing the arrangement of a display control apparatus according to an embodiment of the present invention;

Fig. 2 is a block diagram showing the arrangement of a clock generator of the embodiment shown in Fig. 1;

Fig. 3 is a timing chart showing an example of the timings of a video signal supplied from a computer and dot clock signal in the embodiment shown in Fig. 1;

Fig. 4 is a table for explaining the operation conditions of modules of digital image processing in respective display modes in the display control apparatus of the embodiment shown in Fig. 1; and

Fig. 5 is a flow chart showing the processing of a display mode dependence controller of the embodiment shown in Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention will be described in detail hereinafter with reference to the accompanying drawings.

Fig. 1 is a block diagram showing the arrangement of a display control apparatus according to an embodiment of the present invention.

Referring to Fig. 1, reference numeral 1 denotes a display interface; 2, a video signal processor; 3, a digital image processor; and 4, an FLC display unit. Reference numeral 11 denotes an input terminal for receiving an RGB signal from, e.g., a computer 100 such as a workstation, a personal computer, or the like; 12, a terminal for receiving an image synchronizing signal from, e.g., the computer 100 as in the input terminal 11. The video and synchronizing signals output from the computer 100 are input to and processed by the display interface 1, and thereafter, an image is displayed on the display unit 4.

A display mode detector 15 receives vertical and horizontal synchronizing signals in the computer synchronizing signal input from the terminal 12, and discriminates the current display mode on the basis of the timings, polarities, and the like of these synchronizing signals. The display mode detector 15 supplies the detection result to a display mode dependence controller 17. A clock generator 14 receives a horizontal synchronizing signal in the synchronizing signal supplied from the computer 100, and generates a dot clock signal 41 in accordance with the discrimination result of the display mode supplied from the display mode dependence controller 17.

An ADC (A/D converter) 13 samples an RGB analog signal input from the input terminal 11 at the timing of the dot clock signal 41 supplied from the clock generator 14 to generate a quantized digital RGB image data including 1,280 pixels per line. An interpolation processing circuit 16 expands the image defined by the input digital RGB image data input from the ADC 13 in the vertical direction in correspondence with the display mode. The interpolation processing circuit 16 comprises a line buffer or a frame buffer, and obtains an average of two adjacent pixels as a pixel value therebetween by a linear interpolation method. However, the interpolation processing circuit 16 may adopt other interpolation methods in consideration of the cost/performance. Whether or not interpolation of an image in the vertical direction is performed is designated by the display mode dependence controller 17.

In consideration of the nonlinear input/luminance characteristics (γ characteristics) of a specific or typical CRT, an RGB video signal input from the input terminal 11 normally includes characteristics for canceling the

characteristics. A γ characteristic adjustment circuit 19 adjusts the characteristics included in the RGB image data in correspondence with those of an FLCD panel 24 of the display unit 4, so as to obtain an appropriate luminance on the FLCD panel 24. The γ characteristic adjustment circuit 19 comprises an LUT (look-up table) using a high-speed SRAM, and is set by the display mode dependence controller 17. A halftone processing circuit 21 performs halftone processing (e.g., dither processing) for the image data supplied from the γ characteristic adjustment circuit 19.

A frame change detector 20 compares digital image data supplied from the interpolation processing circuit 16 in units of frames, so as to detect changed lines of the image data between frames, and supplies the detection result to a scanning control circuit 22. The scanning control circuit 22 instructs the display unit 4 to display image data subjected to the halftone processing in the halftone processing circuit 21 on the screen (1,280 x 1,024) of the FLCD panel 24. More specifically, the circuit 22 outputs the line number of a line to be displayed, and then, transfers image data for the line. Thereafter, upon reception of the end message of displaying of the line, the circuit 22 transfers of the line number of the next line to be displayed and image data for the line. Furthermore, the circuit 22 generates a signal for instructing to perform a two-line simultaneous driving operation, as needed. The scanning control circuit 22 changes the scanning method as follows in accordance with an instruction from the display mode dependence controller 17 in correspondence with the display mode.

More specifically, in the VGA mode, the circuit 22 preferentially scans a changed line detected by the frame change detector 20 on the basis of interlace scanning while performing the two-line simultaneous driving operation. On the other hand, in the SVGA mode with the number of pixels (e.g., 800 x 600 or 1,204 x 768) smaller than the number of displayable pixels (1,280 x 1,024) of the FLCD panel 24, the circuit 22 performs a normal one-line driving operation on the basis of an interlace scanning, and preferentially scans a changed line detected by the frame change detector 20 in image data subjected to the interpolation processing. The above-mentioned VGA or SVGA mode is controlled to display an image at substantially the center of the FLCD panel 24 since the number of pixels displayed on the FLCD panel 24 is 1,280 x 960. A display controller 23 displays the image data of a line designated by the scanning control circuit 22 on the FLCD panel 24.

Fig. 2 is a block diagram showing the arrangement of the clock generator 14 of this embodiment.

Reference numeral 32 denotes a phase comparator which detects the phase difference between a horizontal synchronizing signal 31 input from the computer 100 and a signal supplied from a programmable frequency divider 40. A VCO (Voltage Controlled Oscillator) 36 and VCXOs 37 and 38 are oscillators for generating dot clock signal 41 in correspondence with each display mode. LPFs 33 to 35 are low-pass filters having a high-input impedance, each of which filters a frequency signal in corresponding to each of the horizontal frequencies of the respective display modes. Reference numeral 39 denotes a selection switch which comprises a circuit that allows a high-speed operation, such as a low-impedance analog switch, an ECL, or the like. The switch 39 selects one of the outputs from the VCOs (36 to 38) in response to a selection signal 42 supplied from the display mode dependence controller 17, and outputs the selected outputs as the dot clock signal 41.

Fig. 3 is a timing chart showing the relationship between the video signal and the dot clock signal 41.

A frequency division value 43 of the programmable frequency divider 40 is determined and set by the display mode dependence controller 17 so as to generate 1,280 clocks corresponding to the horizontal resolution of the FLCD panel 24 during the horizontal display period, as shown in Fig. 3.

Note that the display mode dependence controller 17 supplies control signals to the video signal processor 2 and the digital image processor 3 in accordance with the discrimination result of the display mode detector 15, as described above.

Examples of the video input signal timings corresponding to the respective display modes and the method of controlling the clock generator 14, the interpolation processing circuit 16, and the scanning control circuit 22 in the respective modes will be explained below with reference to Figs. 1 to 4.

For example, as shown in Fig. 4, when a signal is input in the VGA mode with the number of pixels = 640 x 480, the display mode dependence controller 17 outputs the selection signal 42 for selecting the LPF 33 and the VCO 36, so as to sample the horizontal display period using 1,280 clocks. In this case, the frequency of the dot clock signal 41 is 50 MHz. Since the number of being capable of displaying pixels (1280) in the horizontal direction of the FLCD panel 24 is twice the number of input pixels, the number of pixels to be displayed in the vertical direction is similarly doubled to maintain the aspect ratio. In this case, a control signal for performing the two-line simultaneous driving operation is supplied to the scanning control circuit 22.

On the other hand, when a signal is input in the SVGA mode with the number of pixels = 1,024 x 768, the display mode dependence controller 17 outputs the selection signal 42 for selecting the LPF 35 and the VCXO 38. In this case, the frequency of the dot clock signal 41 is 81.3 MHz (as shown in Fig. 4). Since the number of display pixels in the horizontal direction of the FLCD panel 24 is 1.25 times the number of input pixels, the number of pixels to be displayed in the vertical direction is also multiplied with 1.25 to maintain the aspect ratio, as in the VGA mode. In this case, image data is enlarged in the vertical direction by the interpolation processing circuit 16. For this purpose, the display mode dependence controller 17 supplies a vertical interpolation control signal 26 corresponding to the current mode to the interpolation processing circuit 16.

Furthermore, since the timings of the image synchronizing signals or the frequencies of vertical and horizontal synchronizing signals, dot clock signal, and the like often differ even in a display mode, the display position of an image displayed on the FLCD panel 24 is often displaced from the central portion of the FLCD panel 24. For this reason, the display mode dependence controller 17 supplies control signals to the video signal processor 2 and the digital image processor 3 in response to a display position fine adjustment signal 18 input by a user. For example, since the horizontal displaying period differs if the frequency of the pixel clock signal varies, the width of an image is enlarged or reduced. In order to correct this, the frequency of the dot clock signal 41 must be changed, and the frequency division value 43 of the programmable frequency divider 40 is changed in correspondence with the user's fine adjustment (signal 18). On the other hand, when the horizontal pre-blanking period differs, the start position of displaying in a horizontal direction varies. In order to correct this, the display mode dependence controller 17 supplies a control signal for changing the timing of transfer of image data to the scanning control circuit 22 in response to the user's fine adjustment signal 18.

Fig. 5 is a flow chart showing the processing of the display mode dependence controller 17 of this embodiment.

When the controller 17 receives display mode information detected by and output from the display mode detector 15 in step S1, the flow advances to step S2 to discriminate the detected display mode. If the detected display mode is the VGA mode (640 x 480), the flow advances to step S3, and the controller 17 switches the selection switch 39 to select the LPF 33 and the VCO 36 in the clock generator 14. Then, the controller 17 sets the frequency division value 43 for outputting the dot clock signal 41 of 50 MHz in correspondence with the frequency of 31.5 kHz of the horizontal synchronizing signal in the programmable frequency divider 40. In step S4, the controller 17 instructs the interpolation processing circuit 16 to perform x2 interpolation.

On the other hand, if the detected display mode is the SVGA mode (800 x 600), the flow advances to step S5, and the controller 17 switches the selection switch 39 to select the LPF 34 and the VCXO 37 in the clock generator 14. Then, the controller 17 sets the frequency division value 43 for outputting the dot clock signal 41 of 64 MHz in correspondence with the frequency of 37.8 kHz of the horizontal synchronizing signal in the programmable frequency divider 40. In step S6, the controller 17 instructs the interpolation processing circuit 16 to perform x1.6 interpolation.

Furthermore, if the detected display mode is the SVGA mode (1,024 x 768), the flow advances to step S7, and the controller 17 switches the selection switch 39 to select the LPF 35 and the VCXO 38 in the clock generator 14. Then, the controller 17 sets the frequency division value 43 for outputting the dot clock signal 41 of 81.3 MHz in correspondence with the frequency of 48.3 kHz of the horizontal synchronizing signal in the programmable frequency divider 40. In step S8, the controller 17 instructs the interpolation processing circuit 16 to perform x1.25 interpolation.

Upon completion of the data setting operation in the clock generator 14 and the interpolation processing circuit 16, the flow advances to step S9, and the controller 17 receives the display position fine adjustment signal 18 designated by an operator. In step S10, the controller 17 determines the display position in correspondence with the adjustment signal 18. The flow then advances to step S11, and the controller 17 outputs a control signal to the scanning control circuit 22 to display an image at the determined display position on the FLCD panel 24, thereby controlling the display operation. In this flow chart, instruction outputs to the γ characteristic adjustment circuit 19 and the halftone processing circuit 21 are omitted.

The present invention may be applied to either a system constituted by a plurality of devices or an apparatus consisting of a single device. The present invention may also be applied to a case wherein the invention is attained by supplying a program for practicing the present invention to the system or apparatus. In this case, a storage medium which stores the program according to the present invention constitutes the present invention. By loading the program from the storage medium into the system or apparatus, the system or apparatus operates according to the program.

As described above, according to this embodiment, an image input from a personal computer having various display modes such as VGA, SVGA, and the like can be displayed on the display device by a method suitable for the feature of each video signal.

Since a single interface control board can cope with various display modes, a cost reduction of the display device as a whole can be realized.

In this embodiment, the display interface 1 and the display unit 4 are separately arranged. However, the present invention is not limited to this. For example, the present invention may be applied to a display device which integrates the display interface 1 and the display unit 4.

The present invention can be applied to a system constituted by a plurality of devices or to an apparatus comprising a single device.

Furthermore, the invention is applicable also to a case where the invention is embodied by supplying a program to a system or apparatus. In this case, a storage medium, storing a program according to the invention constitutes the invention. The system or apparatus installed with the program read from the medium realizes the functions according to the invention.

The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore, to apprise the public of the scope of the invention, the following claims are made.

A display control apparatus for displaying an image by receiving an RGB video signal including an image signal and a synchronizing signal receives horizontal and vertical synchronizing signals in the RGB video signal, and detects the current display mode using a display mode detector. A pixel synchronizing clock signal is generated using a clock generator in correspondence with the detected display mode, and the RGB video signal is interpolated by an interpolation processing circuit in correspondence with the display mode and the display screen size of an FLCD panel. The interpolated video signal is subjected to image signal processing, and the processed video signal is displayed on the FLCD panel.

Claims

1. A display control apparatus for displaying an image by receiving a video signal including an image signal and a synchronizing signal, characterized by comprising:

   display mode detection means (15) for detecting a current display mode on the basis of the synchronizing signal in the video signal;

   clock signal generation means (14) for generating a pixel synchronizing clock signal in correspondence with the display mode detected by said display mode detection means;

   interpolation means (16) for interpolating the video signal in correspondence with the display mode and a display screen size of a display; and

   output means (3) for outputting the video signal interpolated by said interpolation means to the display.

2. The apparatus according to claim 1, characterized in that said clock signal generation means comprises a plurality of oscillation means (36 - 38) having different oscillation frequencies, selection means (42) for selecting one of clock signals output from said plurality of oscillation means in correspondence with the display mode, and outputting the clock signal selected by said selection means as the pixel synchronizing clock signal, and frequency division means (40) for frequency dividing the pixel synchronizing clock signal selected by said selection means, and outputs the pixel synchronizing clock signal by locking phases of the clock signal frequency-divided by said frequency division means and a horizontal synchronizing signal.

3. The apparatus according to claim 1, characterized in that said clock signal generation means determines a frequency of the pixel synchronizing clock signal in correspondence with the display screen size of the display and a size of the input video signal.

4. The apparatus according to claim 1, characterized by further comprising A/D conversion means (13) for converting the video signal into a digital signal by sampling the video signal in synchronism with the pixel synchronizing clock signal.

5. The apparatus according to claim 2, characterized in that said frequency division means changes a frequency-division ratio thereof in correspondence with a display position of an image to be displayed on the display.

6. The apparatus according to claim 2, characterized in that said frequency division means changes a frequency division ratio thereof in correspondence with a frequency of the pixel synchronizing clock signal.

7. The apparatus according to claim 2, characterized in that each of said plurality of oscillation means comprises a voltage controlled oscillator.

8. The apparatus according to claim 2, characterized in that said frequency division means changes a frequency-division ratio thereof in correspondence with the display mode detected by said display mode detection means or a manual operation by an operator.

9. The apparatus according to claim 1, characterized in that the display mode includes one of a VGA mode and an SVGA mode.

10. The apparatus according to claim 1, characterized by further comprising gamma correction means (19) for performing gamma correction of the video signal interpolated by said interpolation means.

11. The apparatus according to claim 10, characterized by further comprising halftone processing means (21) for performing a halftone processing for the video signal gamma-corrected by said gamma correction means.

12. The apparatus according to claim 1, characterized in that the display is a display using a ferroelectric liquid crystal.

13. The apparatus according to claim 12, characterized by further comprising scanning control means (22) for instructing a scanning line to be displayed of the display, and thereafter, outputting a video signal to be displayed on the line to the display.

14. A display device for displaying an image by receiving a video signal including an image signal and a synchronization signal, characterized by comprising:

   display mode detection means (15) for detecting a current display mode on the basis of the synchronizing signal in the video signal;

   clock signal generation means (14) for generating a pixel synchronizing clock signal in corre-

spondence with the display mode detected by said display mode detection means;

interpolation means (16) for interpolating the video signal in correspondence with the display mode and a display screen size of a display; and

display means (41) for displaying the video signal interpolated by said interpolation means on a screen.

15. The device according to claim 14, characterized in that said clock signal generation means comprises a plurality of oscillation means (36 - 38) having different oscillation frequencies, selection means (42) for selecting one of clock signals output from said plurality of oscillation means in correspondence with the display mode, and outputting the clock signal selected by said selection means as the pixel synchronizing clock signal, and frequency-division means (40) for frequency dividing the pixel synchronizing clock signal selected by said selection means, and outputs the pixel synchronizing clock signal by locking phases of the clock signal frequency divided by said frequency division means and a horizontal synchronizing signal.

16. The device according to claim 14, characterized by further comprising A/D conversion means (13) for converting the video signal into a digital signal by sampling the video signal in synchronism with the pixel synchronization clock signal.

17. The device according to claim 15, characterized in that each of said plurality of oscillation means comprises a voltage controlled oscillator.

18. The device according to claim 15, characterized in that said frequency division means (40) changes a frequency division ratio thereof in correspondence with the display mode detected by said display mode detection means or a manual operation by an operator.

19. The device according to claim 14, characterized in that the display mode includes one of a VGA mode and an SVGA mode.

20. The device according to claim 14, characterized by further comprising gamma correction means (19) for performing gamma correction of the video signal interpolated by said interpolation means.

21. The device according to claim 20, characterized by further comprising halftone processing means for performing halftone processing for the video signal gamma-corrected by said gamma correction means.

22. The device according to claim 14, characterized in that said display device (41) is a display using a ferroelectric liquid crystal.

23. The device according to claim 22, characterized by further comprising scanning control means for instructing a scanning line to be displayed on the screen, and thereafter, outputting a video signal to be displayed on the line to the screen.

24. A display control method for a display device for displaying an image by receiving a video signal including an image signal and a synchronizing signal, characterized by comprising the steps of:

detecting a current display mode on the basis of the synchronizing signal in the video signal;

generating a pixel synchronizing clock signal in correspondence with the detected display mode;

interpolating the video signal in correspondence with the display mode and a display screen size; and

displaying the interpolated video signal on the display screen.

25. A display control method for displaying an image by receiving a video signal including an image signal and a synchronizing signal, characterized by comprising the steps of:

detecting a current display mode on the basis of horizontal and vertical synchronizing signals in the video signal;

generating a pixel synchronizing clock signal in correspondence with the detected display mode;

interpolating the video signal in correspondence with the display mode and a display screen size of a display; and

outputting the interpolated video signal to the display.

FIG. 1

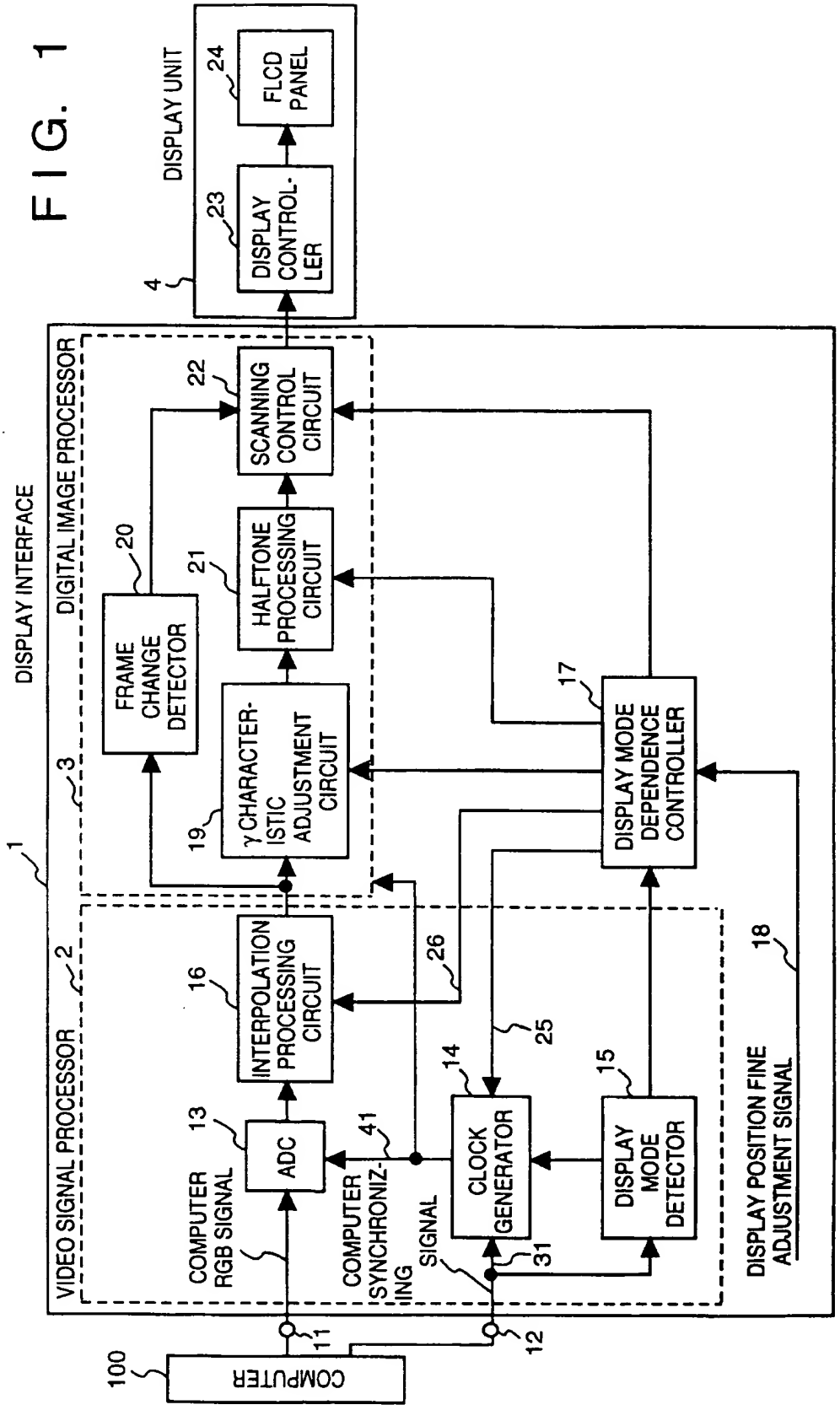
DISPLAY INTERFACE
1
VIDEO SIGNAL PROCESSOR
2
DIGITAL IMAGE PROCESSOR
3
DISPLAY UNIT
4
100
COMPUTER
11
12
COMPUTER RGB SIGNAL
COMPUTER SYNCHRONIZING SIGNAL
13
ADC
41
16
INTERPOLATION PROCESSING CIRCUIT
26
19
γ CHARACTERISTIC ADJUSTMENT CIRCUIT
20
FRAME CHANGE DETECTOR
21
HALFTONE PROCESSING CIRCUIT
22
SCANNING CONTROL CIRCUIT
23
DISPLAY CONTROLLER
24
FLCD PANEL
14
CLOCK GENERATOR
25
31
15
DISPLAY MODE DETECTOR
17
DISPLAY MODE DEPENDENCE CONTROLLER
18
DISPLAY POSITION FINE ADJUSTMENT SIGNAL

FIG. 2

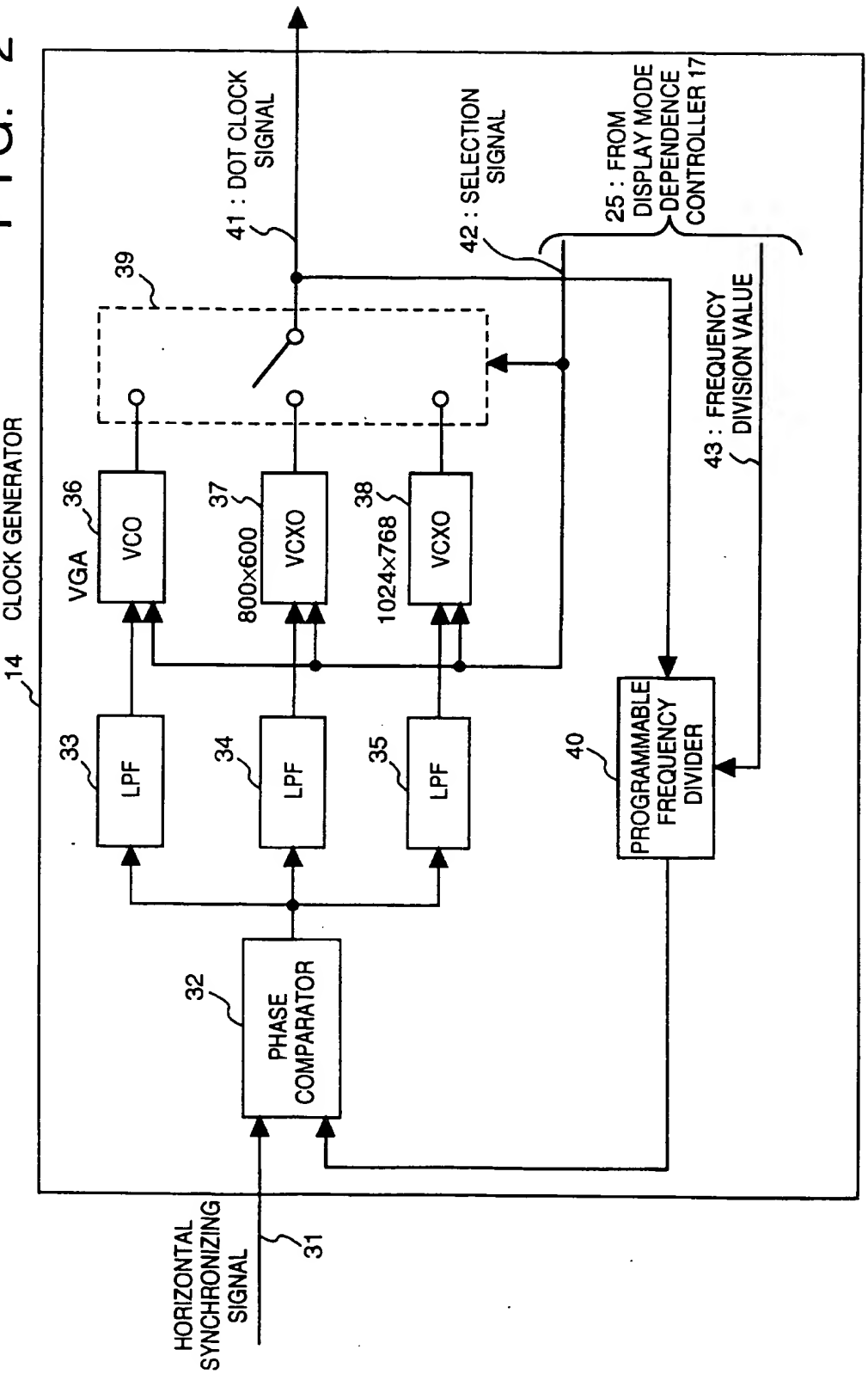
14 CLOCK GENERATOR
41 : DOT CLOCK SIGNAL
42 : SELECTION SIGNAL
25 : FROM DISPLAY MODE DEPENDENCE CONTROLLER 17
43 : FREQUENCY DIVISION VALUE
39
VGA
36
VCO
800x600
37
VCXO
1024x768
38
VCXO
33
LPF
34
LPF
35
LPF
40
PROGRAMMABLE FREQUENCY DIVIDER
32
PHASE COMPARATOR
HORIZONTAL SYNCHRONIZING SIGNAL
31

FIG. 3

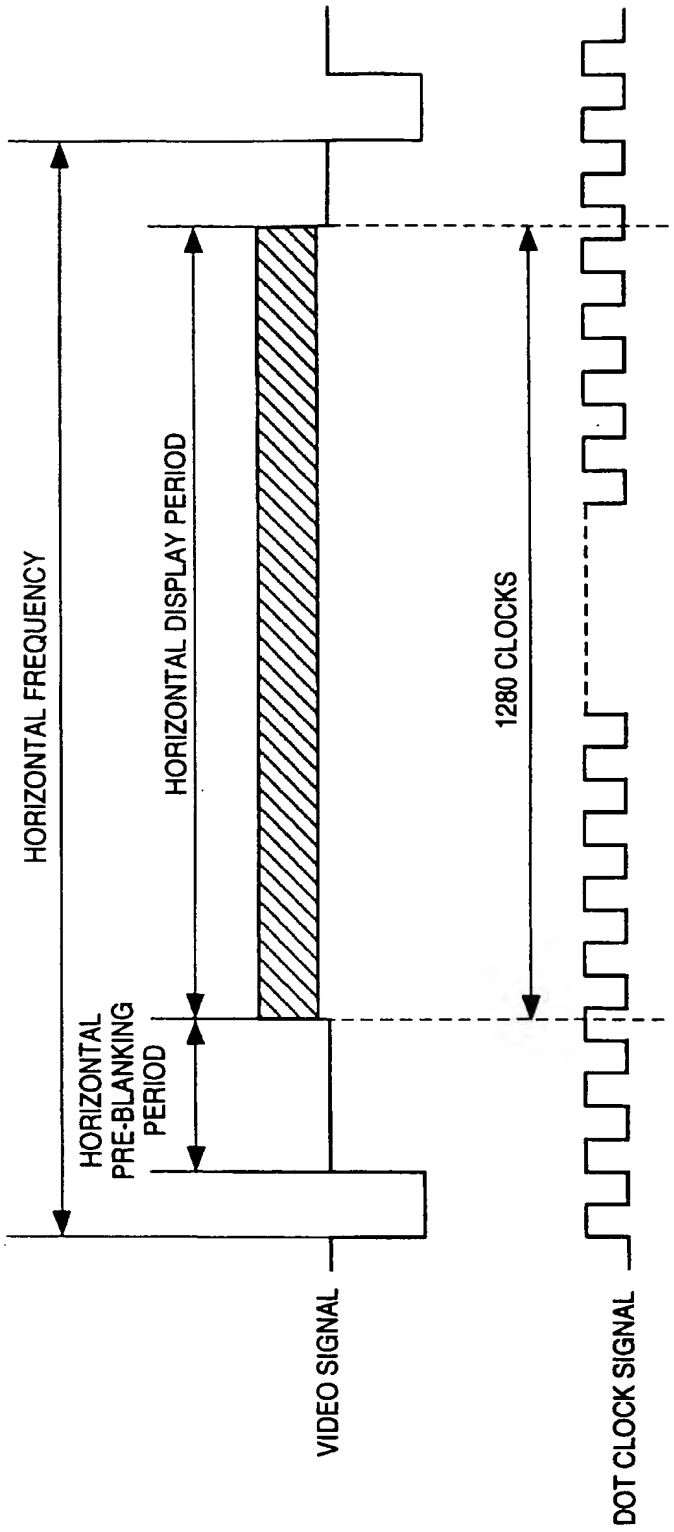
HORIZONTAL FREQUENCY
HORIZONTAL DISPLAY PERIOD
HORIZONTAL PRE-BLANKING PERIOD
1280 CLOCKS
VIDEO SIGNAL
DOT CLOCK SIGNAL

FIG. 4

INPUT SIGNAL (NUMBER OF PIXELS)	VERTICAL FREQUENCY	HORIZONTAL FREQUENCY	FREQUENCY OF PIXEL CLOCK	NUMBER OF DISPLAY PIXELS ON FLCD 24	VERTICAL ENLARGEMENT METHOD	FREQUENCY OF DOT CLOCK SIGNAL
VGA (640 × 480)	60Hz	31.5KHz	25MHz	1280 × 960	× 2 INTERPOLATION	50MHz
SVGA (800 × 600)	60Hz	37.8KHz	40MHz	1280 × 960	× 1.6 INTERPOLATION	64MHz
SVGA (1024 × 768)	60Hz	48.3KHz	65MHz	1280 × 960	× 1.25 INTERPOLATION	81.3MHz

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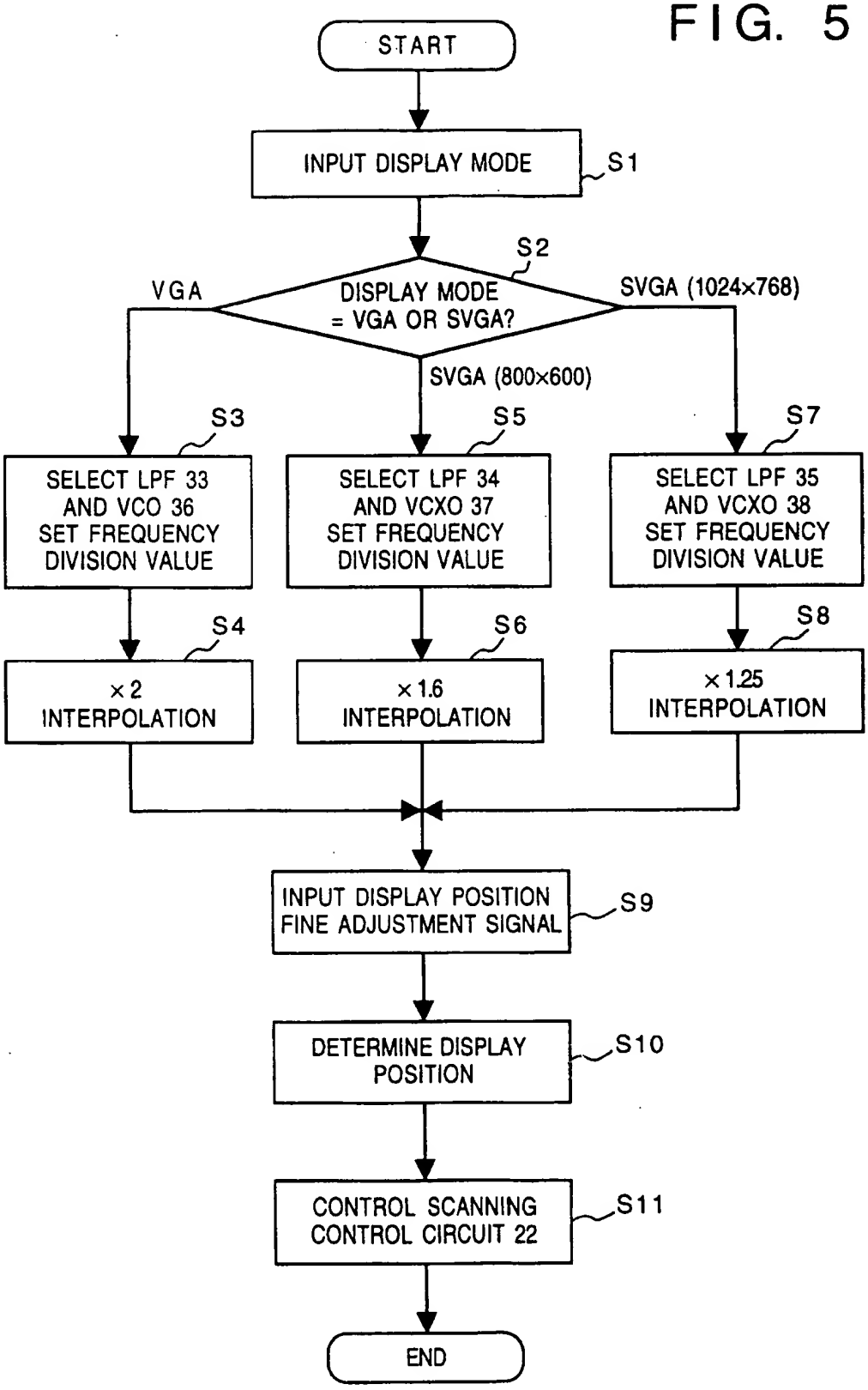
FIG. 5


START
INPUT DISPLAY MODE
S1
S2
DISPLAY MODE = VGA OR SVGA?
VGA
SVGA (800×600)
SVGA (1024×768)
S3
SELECT LPF 33 AND VCO 36 SET FREQUENCY DIVISION VALUE
S4
×2 INTERPOLATION
S5
SELECT LPF 34 AND VCXO 37 SET FREQUENCY DIVISION VALUE
S6
×1.6 INTERPOLATION
S7
SELECT LPF 35 AND VCXO 38 SET FREQUENCY DIVISION VALUE
S8
×1.25 INTERPOLATION
INPUT DISPLAY POSITION FINE ADJUSTMENT SIGNAL
S9
DETERMINE DISPLAY POSITION
S10
CONTROL SCANNING CONTROL CIRCUIT 22
S11
END

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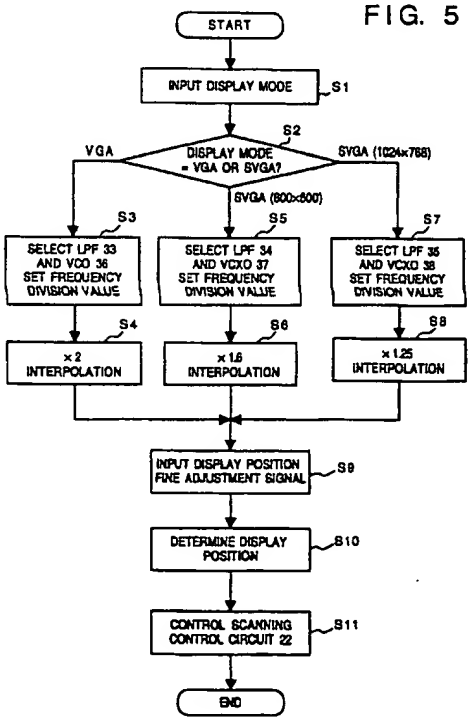
(54) Display mode detector, pixel clock synchroniser and interpolator for ferroelectric liquid crystal display

(57) A display control apparatus for displaying an image by receiving an RGB video signal including an image signal and a synchronizing signal receives horizontal and vertical synchronizing signals in the RGB video signal, and detects the current display mode using a display mode detector. A pixel synchronizing clock signal is generated using a clock generator in correspondence with the detected display mode, and the RGB video signal is interpolated by an interpolation processing circuit in correspondence with the display mode and the display screen size of an FLCD panel. The interpolated video signal is subjected to image signal processing, and the processed video signal is displayed on the FLCD panel.

FIG. 5



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EUROPEAN SEARCH REPORT

Application Number
EP 95 11 6047

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 519 744 A (CANON KK) 23 December 1992 * column 2; claims 2,... * * sections (3.3), (4.2) ; figures 5,6,8 * * column 13, line 45 - line 51 * ---	1,3,4, 9-14,16, 19-25	G09G3/36 G09G5/18 H03L7/099
X	EP 0 400 286 A (GRUNDIG EMV) 5 December 1990 * abstract; claims 1,2 * * column 3, paragraph 1 - paragraph 2 * ---	1,14,24, 25	
A	EP 0 479 508 A (SHARP KK) 8 April 1992 * column 6, line 36 - column 7, line 14; figure 4 * * column 8, line 27 - line 40 * * column 11, line 33 - column 13, line 14 * ---	1,14,24, 25	
A	BROADCAST SESSIONS, MONTREUX, JUNE 10 - 15, 1993, no. SYMP. 1993, 10 June 1993, POSTES;TELEPHONES ET TELEGRAPHES SUISSES, pages 52-62, XP000385280 LACOSTE J P ET AL: "ASPECT RATIO MANAGEMENT IN CCD CAMERAS" * page 55, paragraph 2 * * page 57, paragraph 5 - paragraph 6 * * page 56, line 20 - line 25 * ---	1,14,24, 25	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G H03L G06F H04N
P,A	US 5 389 898 A (TAKETOSHI OSAMU ET AL) 14 February 1995 * abstract * ---	2,15	
A	& JP 06 104 748 A (MATSUSHITA ELECTRIC IND) 15 April 1994 --- -/--	2,15	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 June 1997	Verhoof, P

CATEGORY OF CITED DOCUMENTS

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	SID INTERNATIONAL SYMPOSIUM - DIGEST OF TECHNICAL PAPERS, SEATTLE, MAY 16 - 21, 1993, vol. 24 PART 1, 16 May 1993, SOCIETY FOR INFORMATION DISPLAY, pages 7-10, XP000470741 OHI S ET AL: "4.1: A 13.-DIAGONAL FULL-COLOR HIGH-RESOLUTION TFT-LCD WITH A NEW ANALOG SIGNAL CONVERSION SCHEME" * abstract * -----	10,20	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

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